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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,350	03/07/2001	Chun Hsiang Lai	JCLA6643	4896

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/801,350	LAI ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (5,982,601).

Lin teaches in figures 6 and 9 and related text an electrostatic discharge (ESD) protection circuit, comprising: a silicon controlled rectifier (SCR) circuit (see figure 6 for clarity), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad (Anode) and a ground voltage (Cathode), so as to discharge the electrostatic charges; and

an anti-latch-up circuit 61, which comprises a fourth connection terminal directly connected to a voltage source VH (see figure 6A), a fifth connection terminal coupled to the ground voltage VL, and a sixth connection terminal A connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation.

Regarding claim 3, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/0 pad 1; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line).

Regarding claims 4 and 13, Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region, wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Quigley (5,781,388) in view of Lin (5,982,601).

Regarding claims 1 and 13, Quigley teaches in figure 1 an electrostatic discharge (ESD) protection circuit, suitable for use on the I/0 pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit 22, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage Vss, so as to discharge the electrostatic charges; and

an anti-latch-up circuit RC 17, 18, which comprises a fourth connection terminal directly connected to a voltage source (the pad line), a fifth connection terminal coupled to the ground voltage Vss, and a sixth connection terminal 21 connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation.

Although Quigley does not state a voltage source, this feature is inherent in Quigley's device as the line connected to the pad is the voltage source to the device.

Furthermore, capacitor C also provides a voltage source to the device. Note that the device would not function without a voltage source.

Quigley does not explicitly state that the voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit, and wherein the fourth connection terminal is directly connected to a voltage source.

Lin teaches in figures 6, 9 and 10 and related text a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation, wherein the fourth connection terminal is directly connected to a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation and to directly connect the fourth connection terminal to a voltage source, in Quigley's device, in order to improve the protection capabilities of the device, and in order to simplify the construction of the device, respectively.

Regarding claims 3 and 4, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate

and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;
a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/0 pad 1; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line),

wherein Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Quigley's device as taught by Lin, in order to improve the protection capabilities of the device.

Regarding claim 15, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time

of an ESD pulse in Quigley's device in order to improve the protection capabilities of the device.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley and Lin, as applied to claim 1 above, and further in view of Ker et al. (5,754,380). Quigley and Lin teach substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the 1/O pad and a voltage source in the device of Quigley and Lin in order to provide better protection for the device against ESD event.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

Lin teach substantially the entire claimed structure, as applied to claim 1 above, including a RC delay time of the anti-latch-up circuit being greater than a voltage rising time of an ESD pulse.

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit being smaller than a voltage rising time of an IC power in Lin's device in order to operate the device in its intended use.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Ker et al. (5,754,380).

Lin teaches substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end,

respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the 1/O pad and a voltage source in Lin's device in order to provide better protection for the device against ESD event.

Response to Arguments

Applicant argues that "based on the examiner's understanding of the Lin reference", since the first connection terminal line and the fourth connection terminal line of the Lin reference should be provided with the same voltage, then "Lin failed to disclose "wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation" of claim 1".

Applicant teaches in figure 4 a first connection terminal 112 of the SCR circuit is connected to an I/0 pad 100, and a fourth connection terminal 126 of the anti-latch-up circuit is coupled to a voltage source Vcc. Figure 4 further depicts that the first connection terminal 112 and the fourth connection terminal 126 are connected to each other via diode 108. These connections are also depicted in figure 5, wherein the first connection terminal of the SCR circuit (the circuit comprising the two transistors and two resistors) is connected to an I/0 pad, and a fourth connection terminal of the anti-latch-up circuit (the RC circuit) is coupled to a voltage source Vcc. That is, the claimed invention also discloses the first and forth terminals are connected to the same voltage

source. Therefore, if Lin fails to disclose the claimed limitation of "wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation", as recited in claim 1, then so does the claimed invention.

Applicant argues that the RC circuit disclosed in claim 4 is different from the connection of Lin' s RC circuit, and not anticipated by Lin, because "According to Lin, the RC circuit is a part of the transient oscillator 61, and comprises a capacitor C2 and a resistor R2 (referring to Fig. 6C). The capacitor C2 is connected between VH (not ground) and a node (connected to a gate of a transistor M2, but not a N+ doped region of the SCR circuit). The resistor R2 is connected between the node and VL (not a voltage source)".

Applicant did not explicitly state which elements of the RC circuit is not anticipated by Lin. Note that the device will not operate without ground and voltage source.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
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